UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,446	07/17/2003	Yuan-Ping Tseng	4667-0102P	9175

2292 7590 11/16/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,446	TSENG ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 17 July 2003.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description:

21a in Fig. 2 (see page 2, line 21).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 6, 13 are objected to because of the following informalities:

In claim 6, line 2, change "replacing" with --another-- for proper antecedence to claim 5; and

In claim 13, line 1, change "The manufacturing process" to --A manufacturing process-- for proper antecedence.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-6, 8-9, 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6,214,641 B1) in view of Deane et al. (US 2002/0064033 A1).

Referring to Figs. 1-6 and column 4, line 56 to column 7, line 42, Akram discloses a method of fabricating a single inline memory module (SIMM) that includes the following features:

- The SIMM (10) is comprised of a circuit board (12) with a plug-type connection (14) that includes a plurality of electrical connections (18) extending from one side and with a plurality of slots (20) that extend through the circuit board (12) as shown in Fig.1;
- Each slot (20) corresponds to a recess (30) (i.e. a socket) formed in the circuit board (12) that is sized and shaped to receive a semiconductor die (32) as shown in Fig. 2;
- Use of the term "semiconductor die" or "semiconductor dice" throughout the specification of Akram implies the formation of memory chips by dicing a semiconductor wafer;
- The semiconductor dice (32) are adhesively attached to the circuit board (12) and bond pads (44) corresponding to the semiconductor dice (32) are electrically connected to traces (46) on the circuit board (12) as described in column 5, lines 21-53;
- The SIMM (10) is tested by inserting the plug-type connection (14) into a test fixture (see column 6, lines 1-6);
- Unacceptable die (32X) as determined from the SIMM (10) testing step are replaced by a known good die (KGD) (35) as shown in Fig. 4 and as described in column 6, lines 7-38; and

- The semiconductor dice (32) can subsequently be sealed with an encapsulating material (66) like epoxy or silicone gel as shown in Fig. 5 and as described in column 6, lines 53-61.

These are all of the limitations set forth in claims 1-3, 5-6, 8-9, 12-16 of the applicant's invention with the exception that Akram does not teach or suggest that the electrical connections (18) are made of gold, which is a limitation set forth in both independent claims 1, 13 of the applicant's invention.

Deane et al. teach a memory module that comprises edge connectors (55 in Fig. 4) that can be constructed out of gold (see paragraph [0027]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings Akram and Deane et al. in order to use gold, as taught by Deane et al., for forming the electrical connections of Akram. Deane et al. recognize that gold has the advantage of having the capability to transmit electrical signals without substantial loss (see paragraph [0027], third sentence).

5. Claims 1, 3-5, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinonaga et al. (US 2002/0025608 A1) in view of Littlebury (US 5,017,187) and Deane et al. (US 2002/0064033 A1).

Referring to Figs. 1-6, paragraphs [0032] to [0042], and paragraphs [0048] to [0052], Shinonaga et al. disclose a method of fabricating a memory module that includes the following features:

- The memory module is formed using a multilayer circuit board (10) with edge terminals (14) formed along one of its sides;
- The multilayer circuit board (10) includes a plurality of chip mount areas (12) provided on a top layer (10a);
- Semiconductor memory chips (15) are fixedly bonded to a corresponding chip mounting area (12);
- The chips (15) are electrically connected to the circuit board (10) by wire bonding;
- The chips (15) are tested using contact pad group (21), which is formed on the circuit board (10), to determine if they are defective (see paragraph [0041]);
- Defective memory chips (15) are replaced with non-tested chips, which are then tested until it is determined that all memory chips are non-defective (see Fig. 6 and paragraph [0051]); and
- The memory chips (15) are subsequently sealed with molding resin (28) (see paragraphs [0042] and [0052]).

These are limitations set forth in claims 1, 3-5, 8-9 of the applicant's invention.

However, Shinonaga et al. do not teach or suggest forming the memory chips by dicing a wafer, which is a limitation set forth in independent claim 1 of the applicant's invention. Further, Shinonaga et al. do not teach or suggest that the edge terminals (14) are made of gold, which is also a limitation set forth in independent claim 1 of the applicant's invention.

Littlebury teaches that memory chips can be formed by dicing them from a semiconductor wafer (see column 4, lines 13-16). Deane et al. teach a memory module that comprises edge connectors (55 in Fig. 4) that can be constructed out of gold (see paragraph [0027]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings Shinonaga et al., Littlebury, and Deane et al. in order to dice a wafer, as taught by Littlebury, to form the memory chips of Shinonaga et al. Littlebury shows that one way to form memory chips is to form them on a wafer and then separate them into individual chips by dicing (see column 4, lines 13-16).

Further, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings Shinonaga et al., Littlebury, and Deane et al. in order to use gold, as taught by Deane et al., for forming the edge terminals of Shinonaga et al. Deane et al. recognize that gold has the advantage of having the capability to transmit electrical signals without substantial loss (see paragraph [0027], third sentence).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6,214,641 B1) and Deane et al. (US 2002/0064033 A1) as applied to claim 3 above, and further in view of Mueller (US 6,560,149 B2).

As shown above, the combination of Akram and Deane et al. have all of the limitations set forth in claim 3 of the applicant's invention. However, this combination

lacks the further limitation to claim 3 set forth in claim 7 of the applicant's invention, which is to repair a bad chip by laser radiation. Mueller teaches that it is known in the art to use a laser beam to program redundant elements of a memory for replacing defective elements like memory cells (see column 1, lines 20-56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Akram, Deane et al., and Mueller in order to use a laser beam, as taught by Mueller, for repairing defective memory cells. Mueller recognizes that it is known in the art to use a laser beam for programming redundant circuitry in memories to replace defective circuitry (see column 1, lines 49-56).

7. Claims 10-11, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6,214,641 B1) and Deane et al. (US 2002/0064033 A1) as applied to claims 1, 13 above, and further in view of Kawamura (US 2002/0001180 A1).

As shown above, the combination of Akram and Deane et al. have all of the limitations set forth in claims 1, 13 of the applicant's invention. However, this combination lacks the further limitation to claim 1 set forth in claims 10-11 of the applicant's invention, which is to include a metal shield for thermally dissipating the memory chips (claim 10) by attaching the shield to the memory chips (claim 11). Further, this combination lacks the further limitation to claim 13 set forth in claims 17 of the applicant's invention, which is to include a metal shield for thermally dissipating the memory chips. Kawamura teaches the use of a cover and heat sink (5) for protecting

components like memory chips (3) mounted on a circuit board (1) that can be formed from metal (see Fig. 2C and paragraph [0036]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Akram, Deane et al., and Kawamura in order to use a metal cover and heat sink, as taught by Kawamura, to protect the SIMM of Akram. Kawamura recognizes that the use of a cover and heat sink has numerous advantages including efficient heat dissipation (see paragraph [0033]) and protection of peripheral components from mechanical shock (see paragraph [0034]).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yew et al. teach a single inline memory module, Lin teaches module testing, and Degani et al. teach a multichip module with gold fingers.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813